



Embedded Stackable PCI Express

A comparison of two competing standards

Version 5 - April, 2008



The PC/104 Consortium's approach:

"PCI/104-Express" module based on
"PCIe/104" stackable PCIe bus



PCIe/104 bus key specs

- 4 x1 PCIe lanes
- 1 x16 PCIe lane (also usable as 2 x8, 2 x4, or 2 SDVO)
- SMBus, possible dual USB option
- Up/down stacking (universal add-in card design)
- Power capability: 3.3V@12W, 5V@84W, 12V@100W
- Connector: 3 banks of 52 pins (156 pins total)
- Validated for PCIe Gen 2 signal integrity
- Uses 120-pin PCI as 2nd bus on PC/104 footprint

PCIe/104 bus 3-bank connector

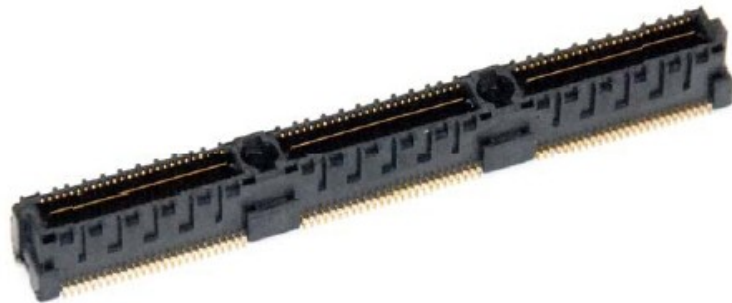


Figure 6-1: Top Connector ASP-129637-03 or equivalent

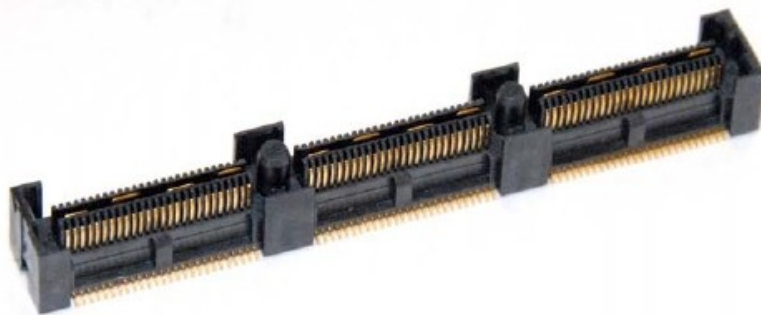
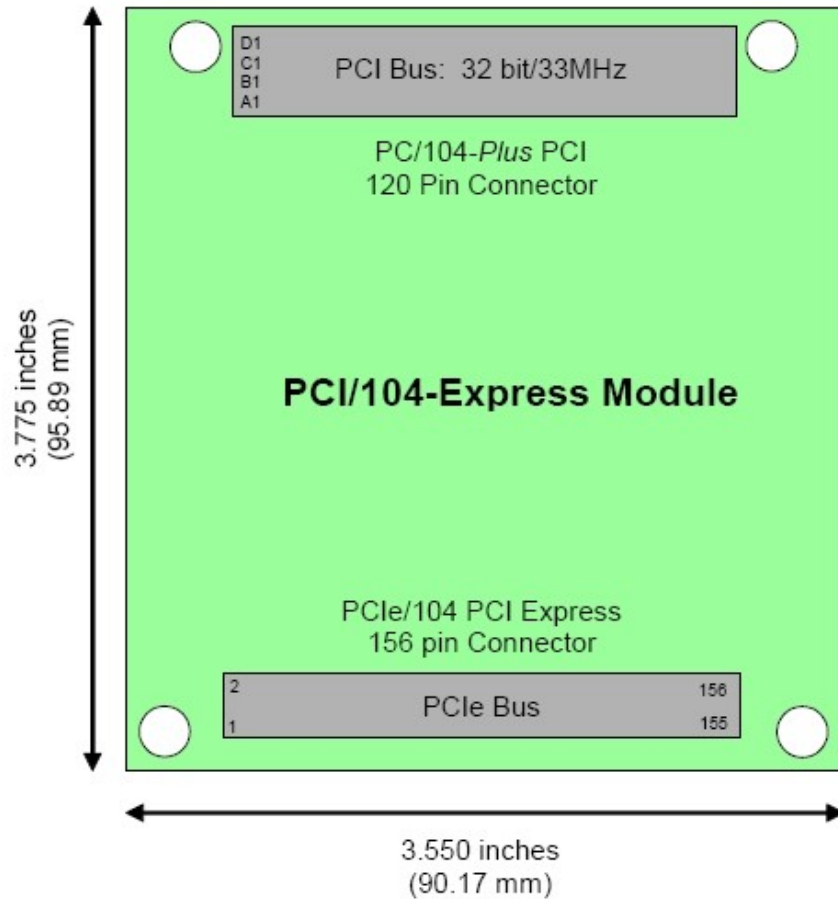


Figure 6-2: Bottom Connector ASP-129646-03 or equivalent

"PCI/104-Express Module" form-factor



PCI/104-Express Module stacking - 1

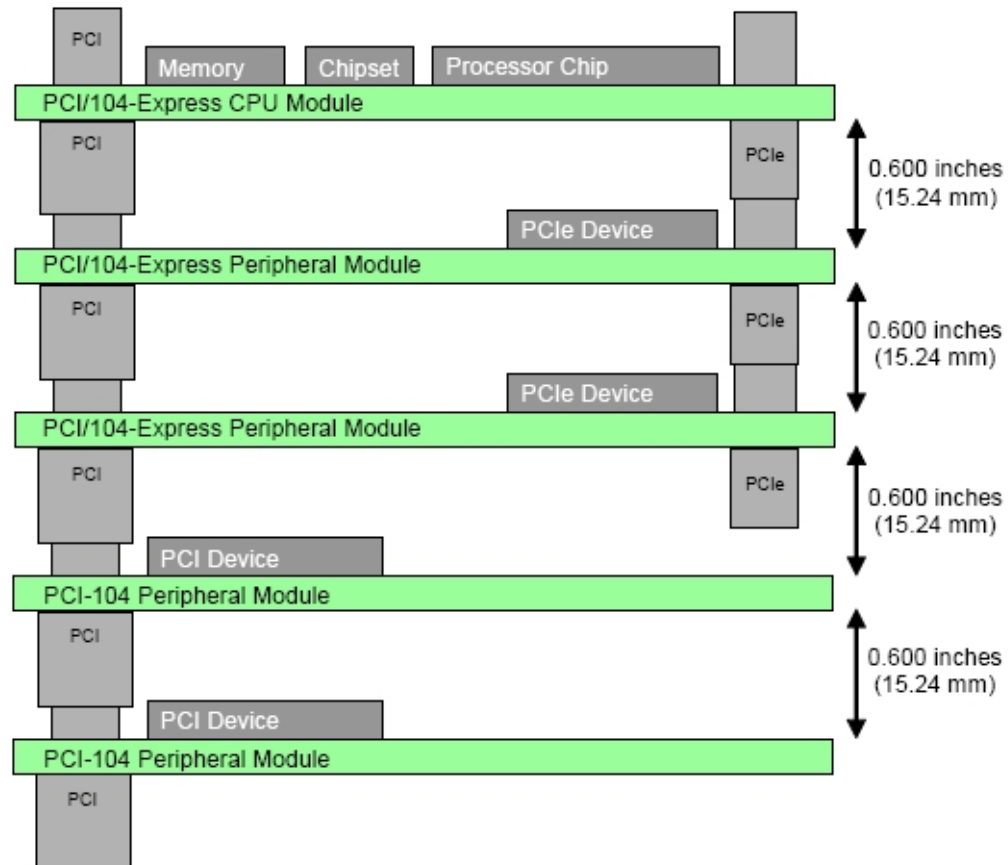


Figure 4-1: Stack-DOWN Configuration Example

PCI/104-Express Module stacking - 2

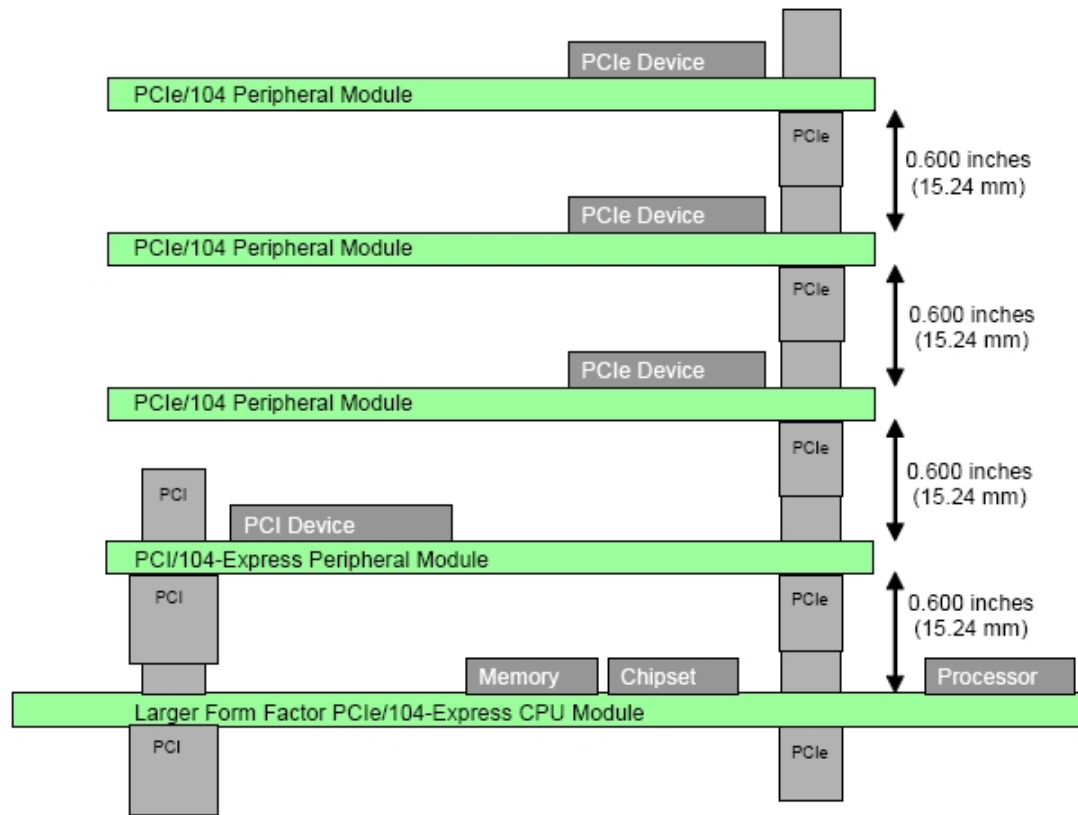


Figure 4-2: Stack-UP Configuration Example with Large Form Factor Host Baseboard

PCIe/104-Express Module stacking - 3

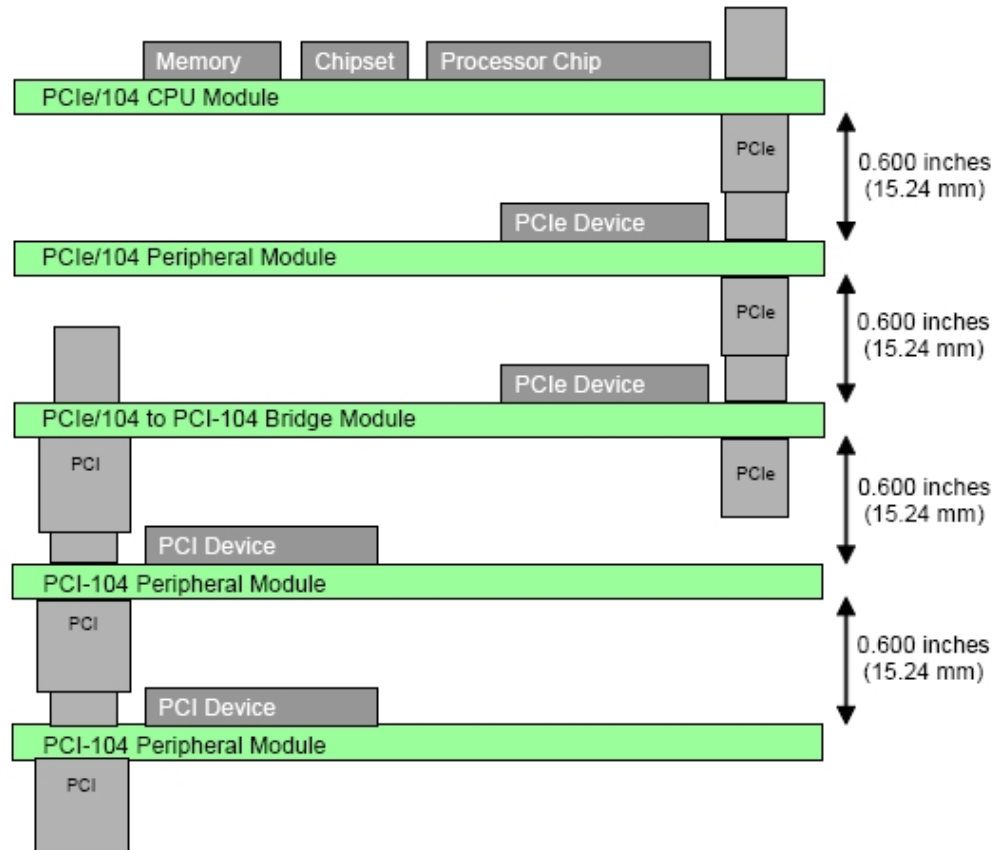


Figure 4-3 PCIe/104 with a PCI Express to PCI Bridge

PCI/104-Express Module stacking - 4

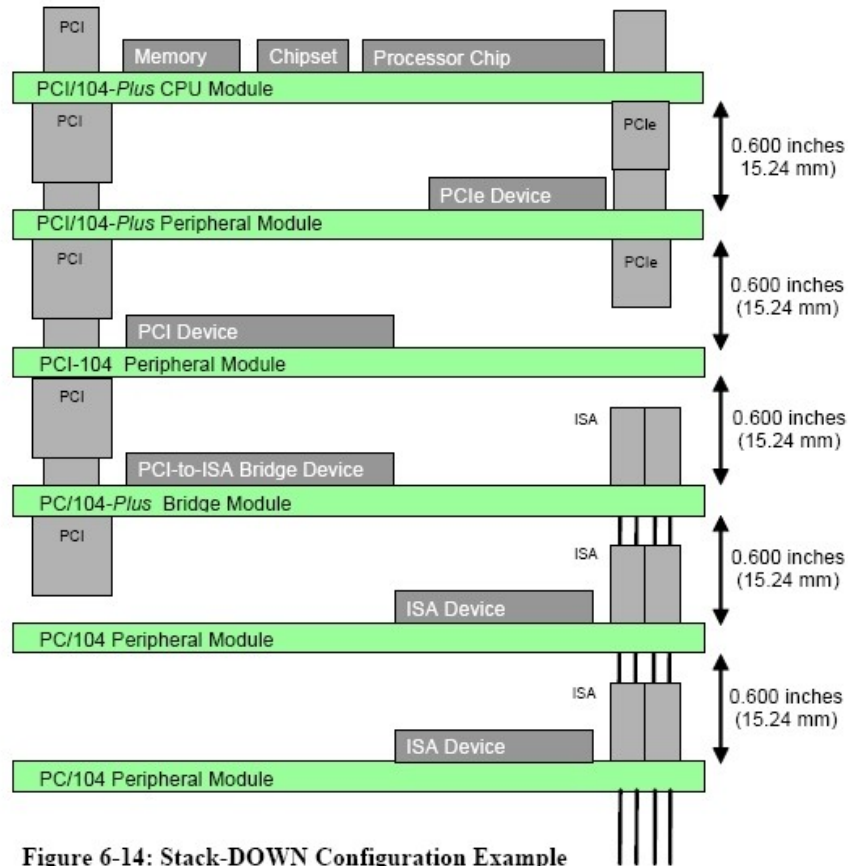


Figure 6-14: Stack-DOWN Configuration Example

PCI/104-Express Module stacking - 5

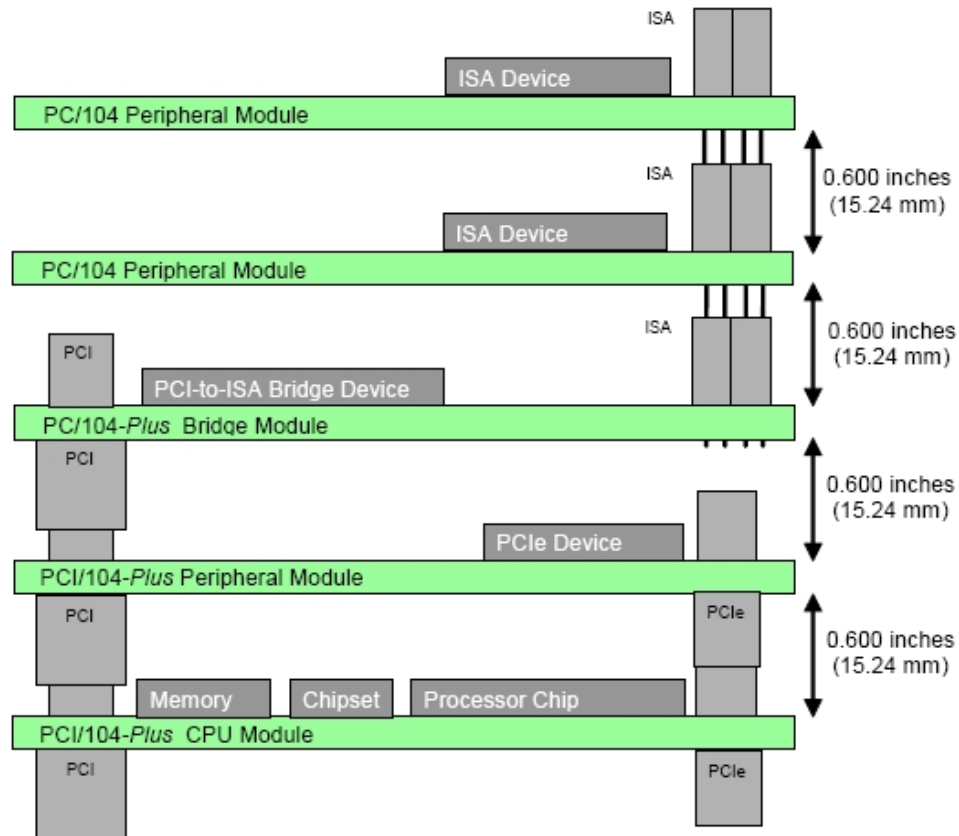


Figure 6-15: Combined Stack-UP Configuration Example



The Small Form Factor Special Interest Group's approach:

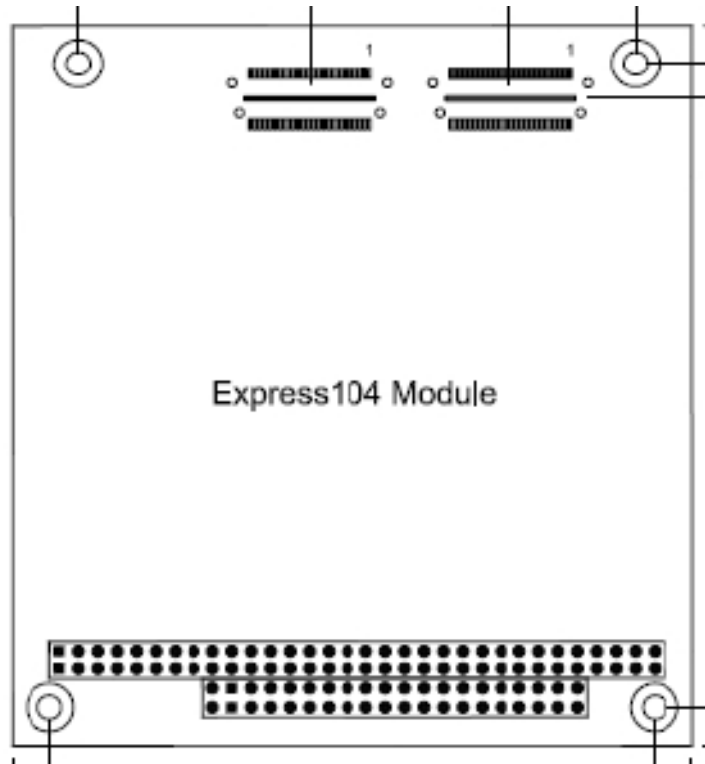
"SUMIT"

(Stackable Unified Module Interconnect Technology)

SUMIT key specs

- 2 x1, 1 x4 PCIe lanes
- LPC bus (with serial IRQ)
- 3 USB 2.0 ports
- SMBus/I2C with SMD alert
- 2 SPI/uWire channels
- 1 ExpressCard channel
- Up-stacking only (but stack can be inverted)
- Power capability: 3V@19W, 5V@56W, 12V@15W
- Connector: 2 banks of 52 pins (104 pins total)
 - Note: single-connector (52-pin) configuration also supported, for 1 x1 and 1 x4 PCIe lanes*
- Validated for PCIe Gen 2 and USB 3.0 signal integrity
- Uses ISA as 2nd bus on PC/104 footprint
- Can coexist with various x16 PCIe expansion buses

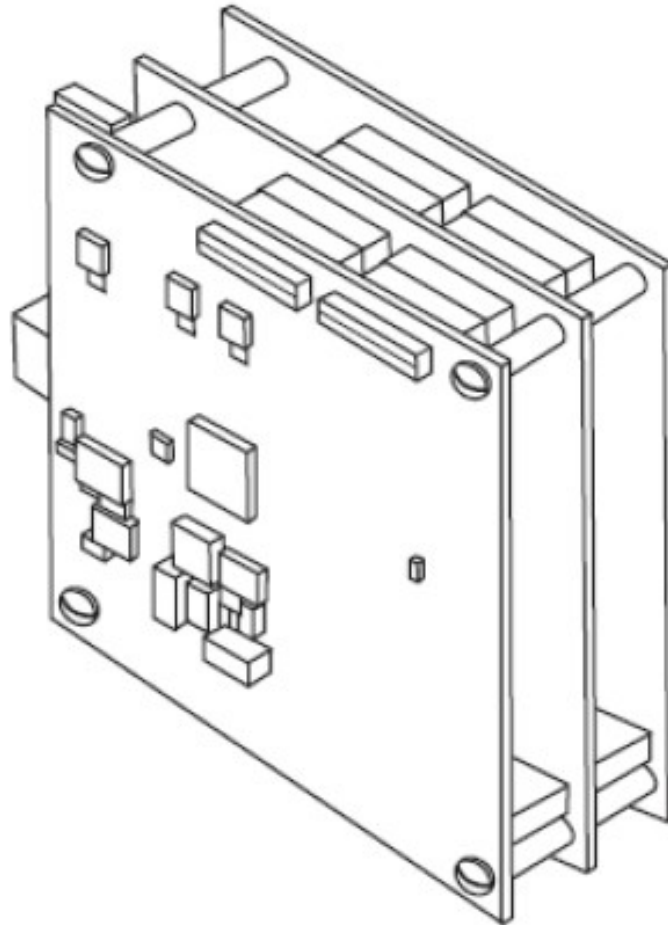
SUMIT "Express104" form-factor diagram



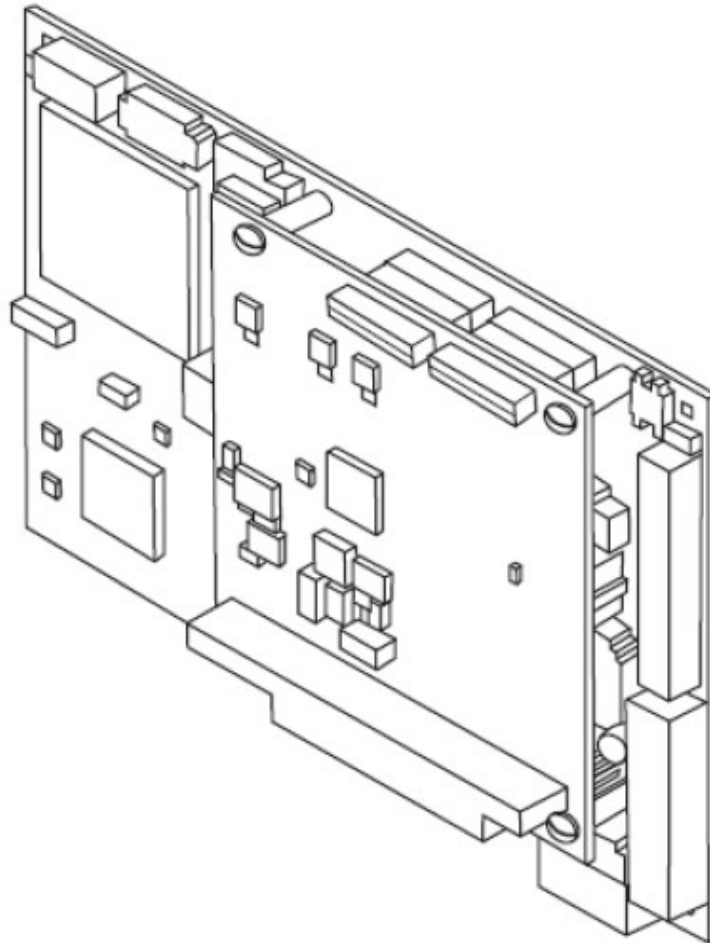
SUMIT "Express104" form-factor photo



SUMIT stacking configurations - 1



SUMIT stacking configurations - 2





Comparing the two stackable embedded PCI Express alternatives

Key feature comparison

Feature	PCIe/104 bus	SUMIT bus
PCIe lanes	4 x1, 1 x16; x16 lane alternately usable as 2 x8, 2 x4, or 2 SDVO	2 x1, 1 x4
LPC bus	No	Yes (with IRQ support)
USB channels	No (2 possible in future)	3
SMBus support	Yes	Yes
SPI channels	No	2
ExpressCard channels	No	1
Companion bus on PC/104 form-factor	120-pin PCI bus	104-pin ISA bus
Stacking options	Up/down	Up only (invertible)
Connectors	One 156-pin connector (three banks of 52 pins)	Two 52-pin connectors



Pros and cons: PC/104 Consortium's PCIe/104 bus

- **Claimed or perceived pros:**
 - x16 lane for high-end networking, graphics, FPGA, DSP...
 - x16 lane configurable as 2 x8, 2 x4, or 2 SDVO
 - Supports up/down stacking (universal add-in card design)
 - Full power management support
- **Perceived cons:**
 - Three-bank bus may require more PCB layers
 - Stack up/down requires PCIe signal switches
 - No legacy ISA support on PCIe/104 bus (no LPC, no IRQ)
 - Currently no USB channels (possibly 2 in future)
 - No SPI support



Pros and cons: SFF-SIG's SUMIT bus

- **Claimed or perceived pros:**
 - Reduced connector footprint with single-bank option
 - Gap between separate A/B connectors aids routing
 - Includes USB, ExpressCard, SPI/uWire I/O buses
 - Includes LPC and IRQ for ISA support
- **Perceived cons:**
 - Lacks x16 lane for bus-based high-end graphics, etc.
 - Max. of 3 PCIe lanes limits bus-based PCIe devices
 - Up-stacking only (but stacks can be inverted)
 - Underutilizes available stacking bus real estate

For further information, visit...

- **PC/104 Consortium -- PC104.org**
- **SFF-SIG -- SFF-SIG.org**

Please note: Specification diagrams appearing in this article are courtesy of their respective parent organizations. Additionally, many of the specification and form-factor names cited above are claimed as trademarks or registered trademarks by their owners; consult the relevant specifications for long lists of claimed marks.

Full disclosure: This article's author, Rick Lehrbaum, wrote the original PC/104 Specification, formed the PC/104 Consortium, and served as the group's initial chairman. Additionally, he was the co-founder of, and currently serves as CTO of, **Ampro Computers Inc.**, which created PC/104 and is a member of both the PC/104 Consortium and the SFF-SIG.