The EPIC Express™ Specification:

Stackable PCI Express™ Expansion for EPIC, The Embedded Platform for Industrial Computing

Version 0.80

August 26, 2005

This specification is a combined technical effort by WinSystems, VersaLogic, Octagon Systems, Micro/sys, and Ampro Corporations to define the stackable PCI Express expansion architecture for the next generation SBC.

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REVISION HISTORY

Revision 0.10 – June 15, 2005
- a. Pre-release, First Pass

Revision 0.20 – July 19, 2005
- a. Pre-release, Second Pass

Revision 0.80 – August 26, 2005
- a. Pre-release, Third Pass

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EPIC Express™ SPECIFICATION

Revision 0.80 – August 26, 2005

1. INTRODUCTION

This document defines the addition of PCI Express, the next generation serial interconnect bus, to the Embedded Platform for Industrial Computing (EPIC). PCI Express was chosen because of its performance, scalability, wide market acceptance, and growing silicon availability worldwide. The PCI Express architecture uses familiar software and configuration interfaces of the conventional PCI bus architecture, but provides a new high-performance physical interface while retaining software compatibility with the existing conventional PCI infrastructure.

PCI Express is a high performance I/O architecture used in both desktop and mobile applications. This hierarchical, point-to-point interconnect works well with on-board and slot oriented architectures. The purpose of this Specification is to adapt it to the stacking-style architecture employed with EPIC. It is the logical evolution of the EPIC specification in that it adds PCI Express expansion capability to this industrial computing platform. The reason for adding PCI Express was to provide a bridge to the future while maintaining legacy support for the vast number of PC/104 expansion modules available worldwide.

An EPIC board with the addition of PCI Express becomes an EPIC Express board. This specification details the type of connector and its placement on an EPIC board and PC/104-based expansion modules. None of the dimensions or I/O zones of an EPIC board change, only the replacement of the parallel PCI bus (as implemented through the PC/104-*Plus* connector) with a serial PCI Express connector. Similarly, the I/O boards that stack on top of EPIC Express are PC/104-size with the PC/104-*Plus* connector removed and replaced with a PCI Express stacking connector.

2. STACKABLE PCI Express Architecture

A PCI Express link can be scaled on a device-by-device basis to meet different I/O controller's bandwidth and application objectives. The PCI Express Base Specification defines the configuration of serial links as x1, x2, x4, x8, x16, and x32. The EPIC Express supports four x1 and two x4 links. This is implemented in two configurations: Standard and Full.

The Standard option is a replacement for existing, standard PC/104-*Plus* devices using four x1 links (A – D). It allows up to four boards to be stacked yet requires only a single 28-pin connector. The connector is about 1/3 the size of a PC/104-*Plus* connector which frees up valuable printed circuit board real estate, quadruples the bandwidth of the link, and eliminates the slot selection switch.

EPIC Express Configuration Options

	Standard	Full
Connector Size	1-bank	3-bank
Links	A, B, C, D	A, B, C, D, E, F
Lane Width	Four x1	Four x1, Two x4
Clocks	A, B, C	A, B, C, D, E, F
Power	+5V, PERST#, 3.3Vaux	+5V, PERST#, 3.3Vaux +12V, -12V

The other configuration supports more bandwidth-intensive controllers and more PCI Express links. It supports the four x1 links on the first connector bank and the two x4 links (E &F) plus more clocks, power and ground. This adds two additional connector banks which take up approximately the same amount of area as a PC/104-*Plus* connector. This is called the Full EPIC Express configuration since it has more capacity and requires a larger connector with three 28-pin banks.

The height of a stack is maintained at 0.662-inches. This permits the same spacers and PC/104 cards to be used. Unlike a PC/104 stack, the stacking order for the EPIC expansion modules is significant. The Full x4 EPIC Express expansion module must be closest to the root SBC. Stacked above that would be any x1 lane modules and finally standard PC/104-compatible modules. Even though the standard and full configurations require different EPIC Express connectors, a 1 bank, Standard EPIC Express Module can plug into a 3-bank, Full EPIC Express Module but not vice versa. The reason is that a 3-bank connector is simply a 1-bank connector replicated two more times in a contiguous housing to support additional pins.

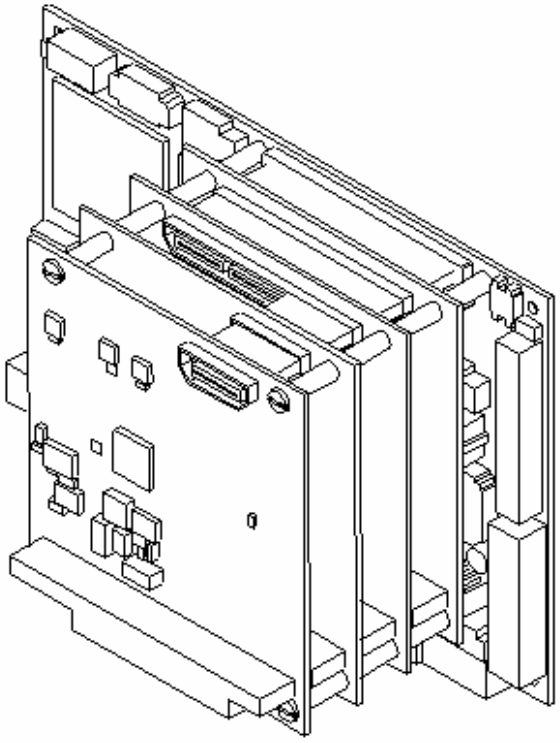


Figure 1. EPIC Express SBC with one Full and two Standard Expansion Cards

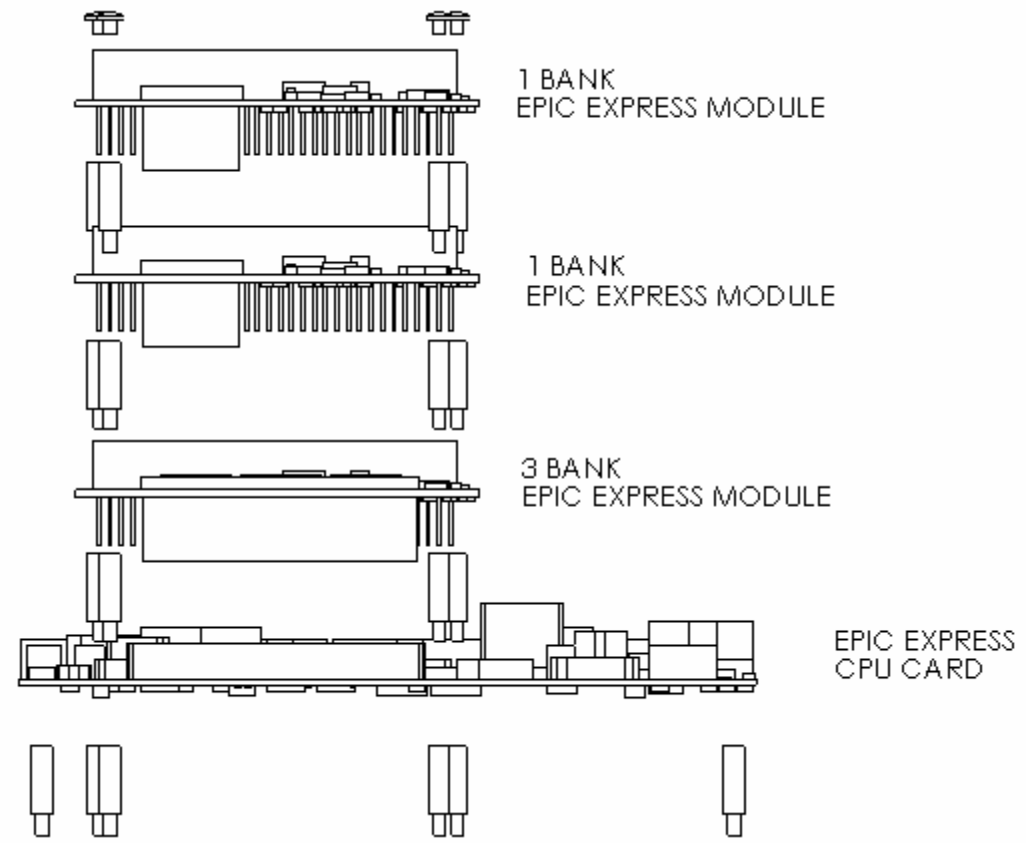
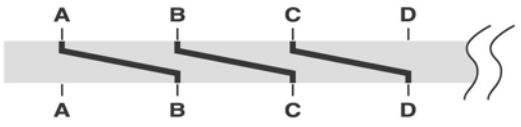
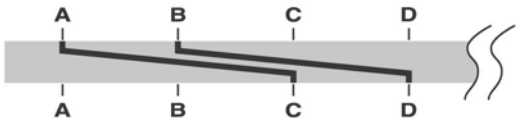


Figure 2. Exploded view of EPIC Express Stack

Automatic Link Alignment – One of the design goals of EPIC Express modules was to not require any jumpers for address or slot alignment. Its stacking design is physically similar to PC/104 and PC/104-*Plus* but the connectors employed are not through-hole style. Those were designed to implement a passive, parallel bus. By contrast, EPIC Express uses a pair of surface mount connectors that allows one or more PCI Express controllers to be mounted on the I/O expansion module. This feature allows automatic link alignment which eliminates the needs for jumpers or special stacking order. Boards not supporting PCI Express simply pass the signals up the stack from one connector to another.



EPIC Express with one I/O device on board

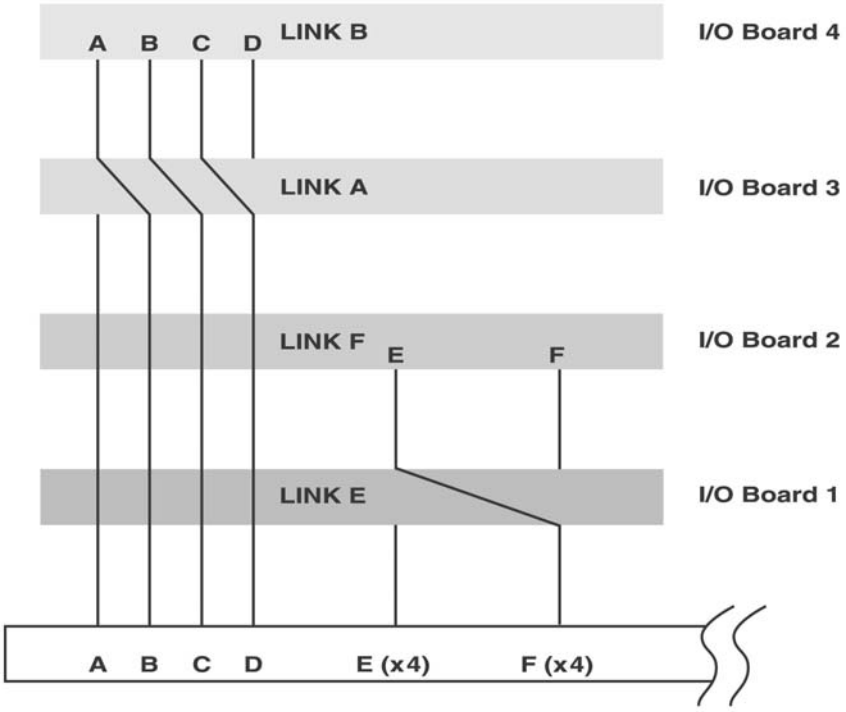


EPIC Express with two I/O devices on board

An EPIC Express module with a single x1 PCI Express controller is always wired to Link A on the bottom side connector its pc board. The top connector will have Link A wired from Link B on the bottom connector. The same methodology is maintained for Links B and C on the top connector since they are wired from Link C and Link D respectively on the bottom connector. Link D on the top connector is not connected.

An EPIC Express module with two x1 PCI Express controllers is always wired to Link A and Link B on the bottom side connector of its pc board. Therefore, Link A and Link B on the top connector will be wired from Link C and Link D respectively on the bottom connector. Link C and Link D on the top side connector will not be connected.

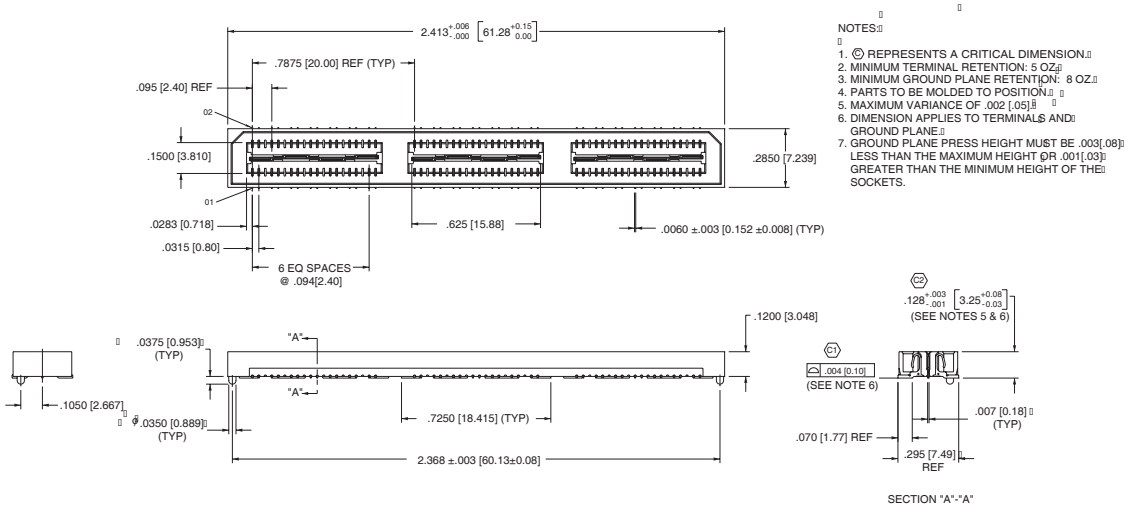
An EPIC Express module with a single x4 PCI Express controller is always wired to Link E on the bottom side connector of its pc board. The top connector will have Link E wired from Link F on the bottom connector. Link F on the top side connector will not be connected. Links A, B, C, and D will be wired from the top connector to the bottom connector since there is not a x1 PCI Express controller on the board.



4 Board Full EPIC Express Stack with two x 4 links and two x 1 links featuring automatic alignment for each.

3. CONNECTOR SPECIFICATION

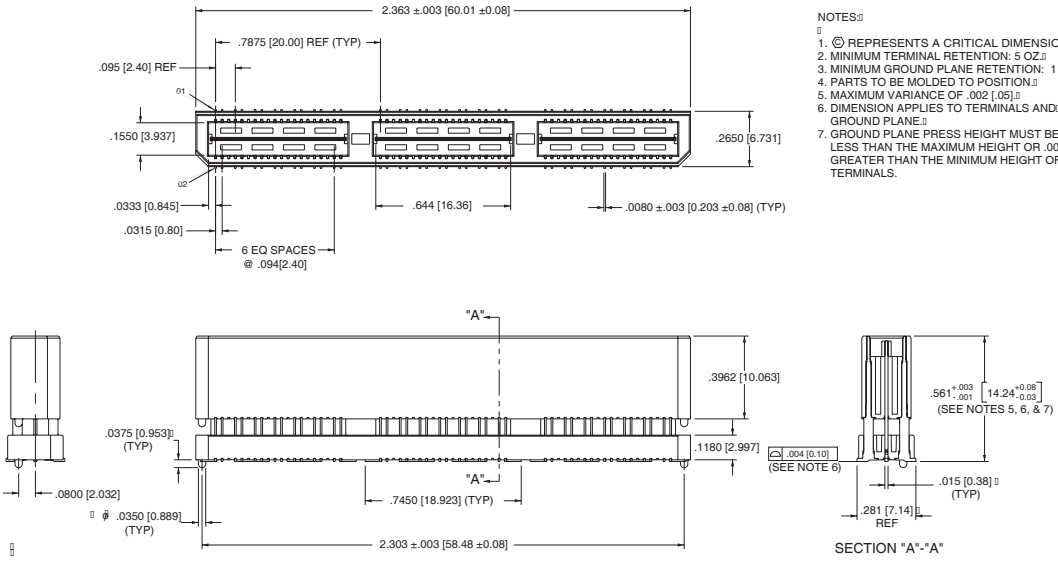
3.1 EPIC Express Top : Three-Bank Connector



NOTES:

1. Ⓒ REPRESENTS A CRITICAL DIMENSION.
2. MINIMUM TERMINAL RETENTION: 5 OZ.
3. MINIMUM GROUND PLANE RETENTION: 8 OZ.
4. PARTS TO BE MOLDED TO POSITION.
5. MAXIMUM VARIANCE OF .002 [.05].
6. DIMENSION APPLIES TO TERMINALS AND GROUND PLANE.
7. GROUND PLANE PRESS HEIGHT MUST BE .003[.08] LESS THAN THE MAXIMUM HEIGHT OR .001[.03] GREATER THAN THE MINIMUM HEIGHT OF THE SOCKETS.

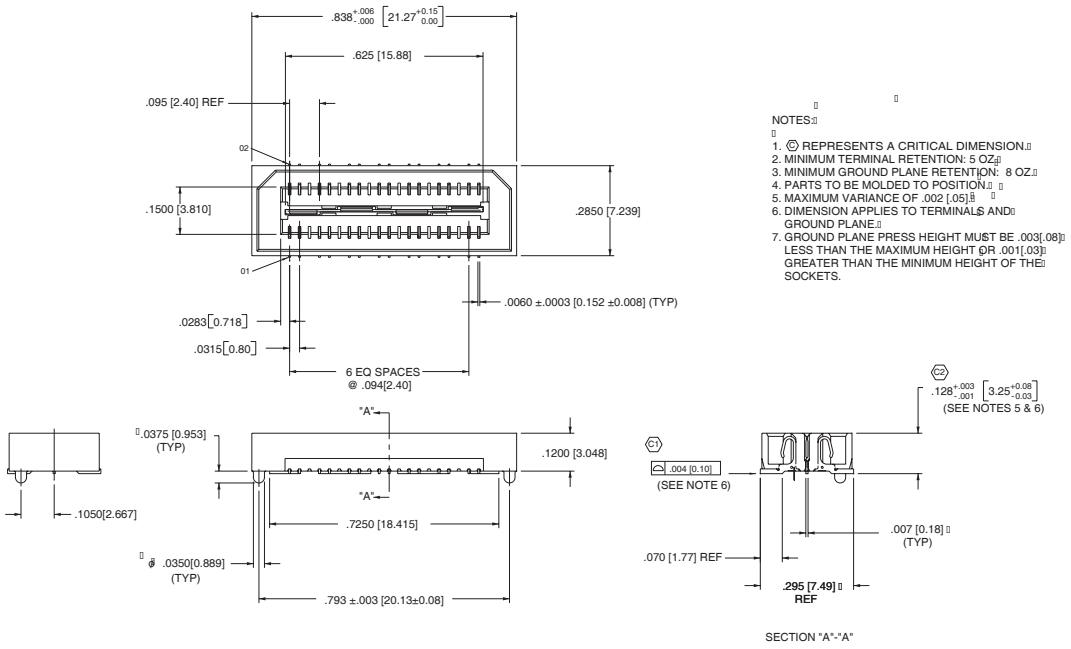
3.2 EPIC Express Bottom : Three-Bank Connector



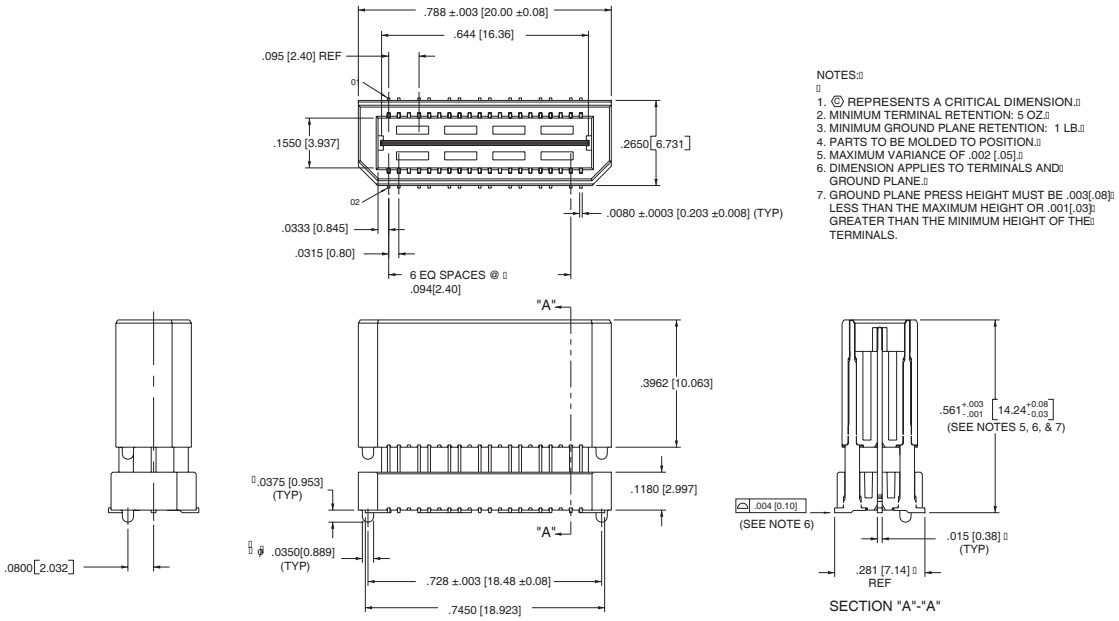
NOTES:

1. Ⓒ REPRESENTS A CRITICAL DIMENSION.
2. MINIMUM TERMINAL RETENTION: 5 OZ.
3. MINIMUM GROUND PLANE RETENTION: 1 LB.
4. PARTS TO BE MOLDED TO POSITION.
5. MAXIMUM VARIANCE OF .002 [.05].
6. DIMENSION APPLIES TO TERMINALS AND GROUND PLANE.
7. GROUND PLANE PRESS HEIGHT MUST BE .003[.08] LESS THAN THE MAXIMUM HEIGHT OR .001[.03] GREATER THAN THE MINIMUM HEIGHT OF THE TERMINALS.

3.3 EPIC Express Top : One-Bank Connector



3.4 EPIC Express Bottom : One-Bank Connector



3.5 EPIC Express Connector Physical Specifications

Materials

Housing:	LCP (Liquid Crystal Polymer) Thermoplastic, UL Rated 94-V0
Contact:	Phosphor Bronze

Contact Finish

Socket Interface:	10 microinches Gold on contact area, 3 microinches min Gold on remainder
Terminal Interface:	10 microinches Gold on contact area, 3 microinches min Gold on rRemainder
Underplate:	50 microinches min Nickel

Mechanical Performance

Insertion Force, One-bank:	5.0 lbs. max.
Insertion Force, Three-bank:	15.0 lbs max.
Withdrawal Force, One-bank:	4.0 lbs. max.
Withdrawal Force, Three-bank:	10.6 lbs. max.
Normal Force:	90 gr. @ 0.006 in.deflection
Durability:	100 Cycles min.
Operating Temp:	-55°C to +125°C

Electrical Performance

Contact Resistance:	29 milliohms max.
GND Resistance:	5.0 milliohms max.
Contact Current Capacity:	2.0 A @ 30°C temp rise
GND Current Capacity:	9.5 A @ 30°C temp rise
Dielectric Strength:	675 VAC
Insulation Resistance:	5,000 MΩ min.

Solderability

Processing Temperature:	260°C Produces no blistering, distortion, or discoloration

High Frequency Performance

Single-Ended System Impedance:	50 Ohms ±10%
Differential Pair System Impedance:	100 Ohms ±10%
Differential Performance:	5 GHz @ -3db insertion loss

3.6 EPIC Express Connector Part Number Information:

Top, Three Bank:	Samtec QSE-042-01-L-D-DP-A or equivalent
Bottom, Three Bank:	Samtec QTE-042-10-L-D-DP-A or equivalent
Top, One Bank:	Samtec QSE-014-01-L-D-DP-A or equivalent
Bottom, One Bank:	Samtec QTE-014-10-L-D-DP-A or equivalent

4. PIN DESCRIPTIONS

EPIC Express follows the naming conventions established for PCI Express to form the root of a pin name, with a prefix added to designate the link. For example, a pin in a given link and lane may be named "A_PETp0" or "A_PERn0":

"A"	designates the link to which a pin is associated
"PE"	designates PCI Express pin functions
"T" or "R"	defines the pin as a transmit or receive pin respectively
"p" or "n"	defines the pin as the positive or negative constituent of a pair
"0"	defines the lane in a link to which the pin belongs

Clocks follow a similar naming convention. For example, "A_CLKp" and "A_CLKn" pins are defined by the following:

"A" - designates the link to which the clock is associated
"CLK" - designates PCI Express clock pin functions
"p" or "n" - defines the pin as the positive or negative constituent of a pair

4.1 Other Pin Functions:

3.3Vaux	positive 3.3 volt auxiliary power
+5V	positive 5 volt power
+12V	positive 12 volt power
-12V	negative 12 volt power
PERST#	Active-low Reset for all PCI Express devices
GND	Ground power, supplied through center pin in each bank

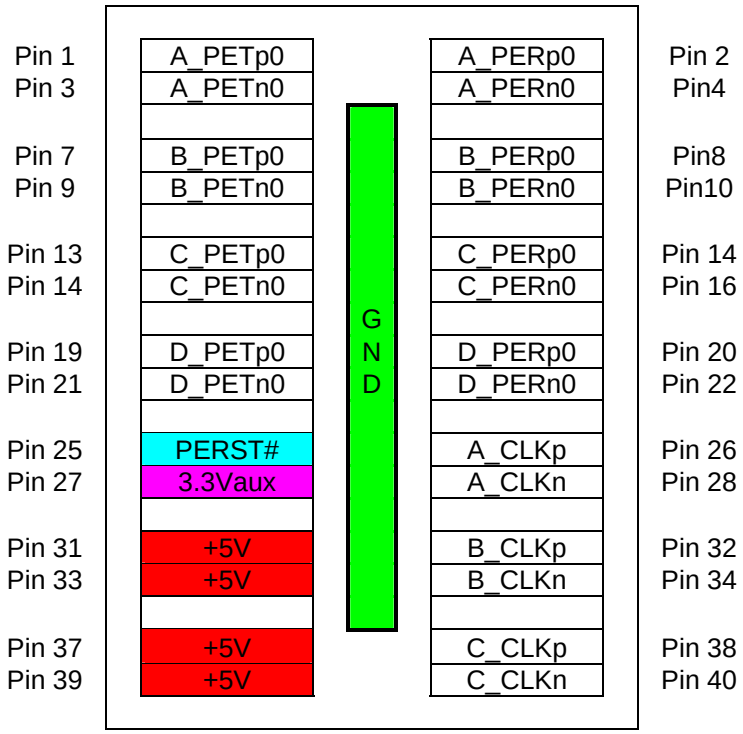
4.2 Pin Functions Not Currently Supported:

+3.3V
SMBus
JTAG
WAKE
Hot-plug Presence detect

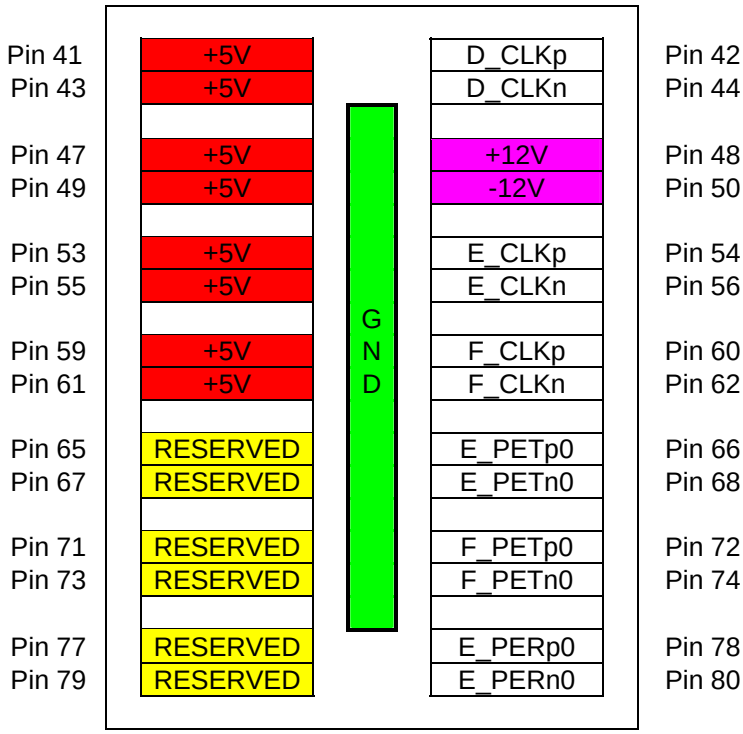
4.3 Reserved Pins

Reserved pin functions will be defined in future releases of this specification and must be left unconnected.

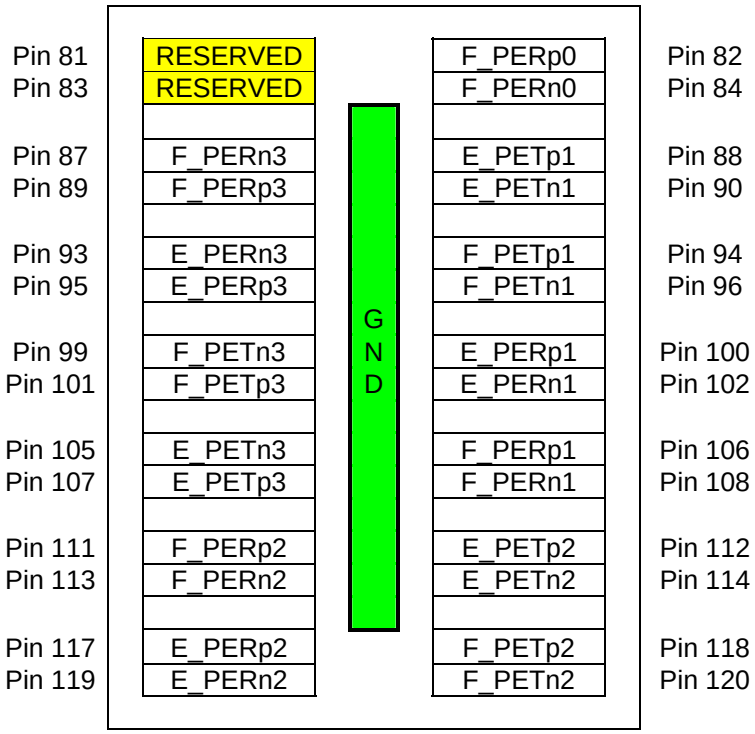
4.4 EPIC Express - Bank One Connector Pin Assignments



4.5 EPIC Express – Bank Two Connector Pin Assignments



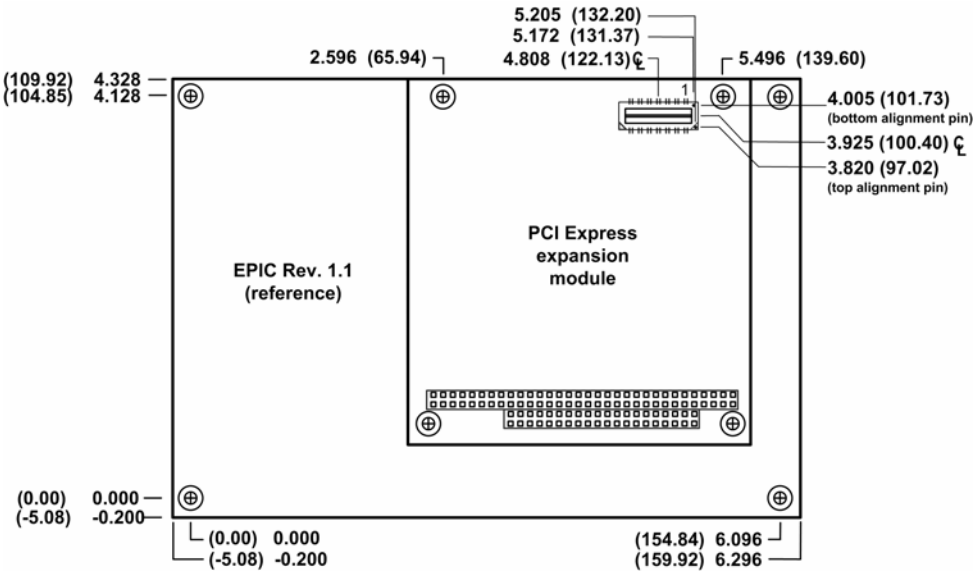
4.6 EPIC Express – Bank Three Connector Pin Assignments



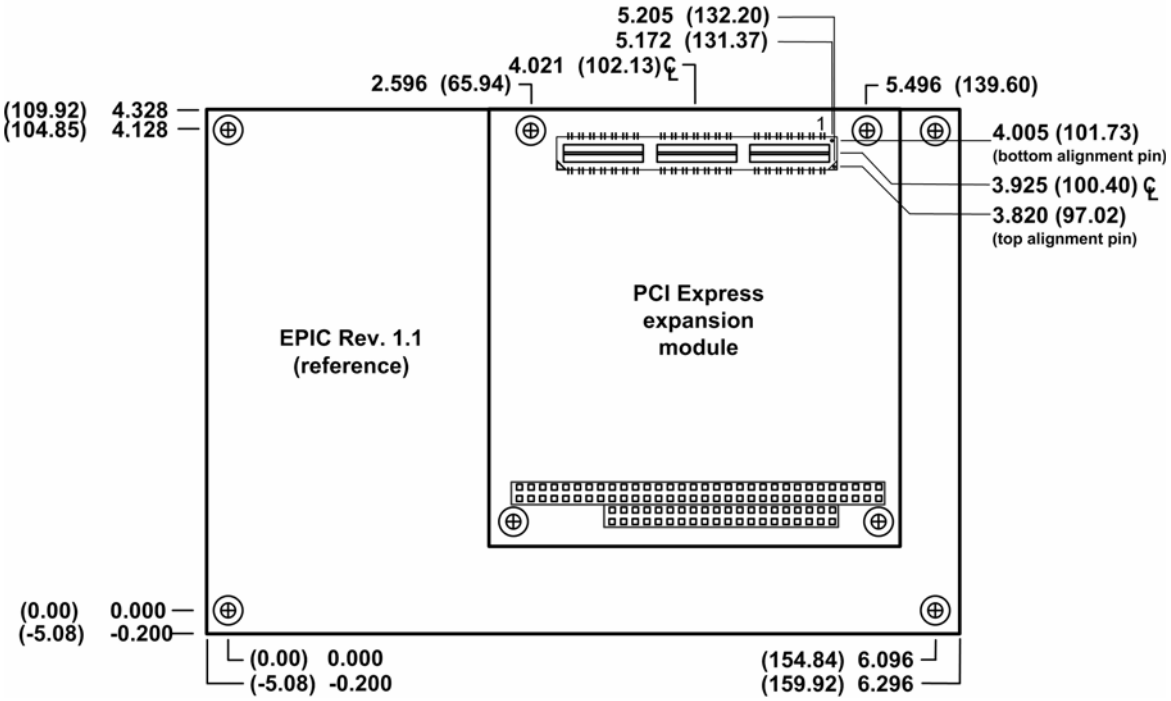
5. MECHANICAL SPECIFICATIONS

All specifications and dimensions, except for those explicitly noted herein for EPIC Express, are defined within their appropriate parent specification.

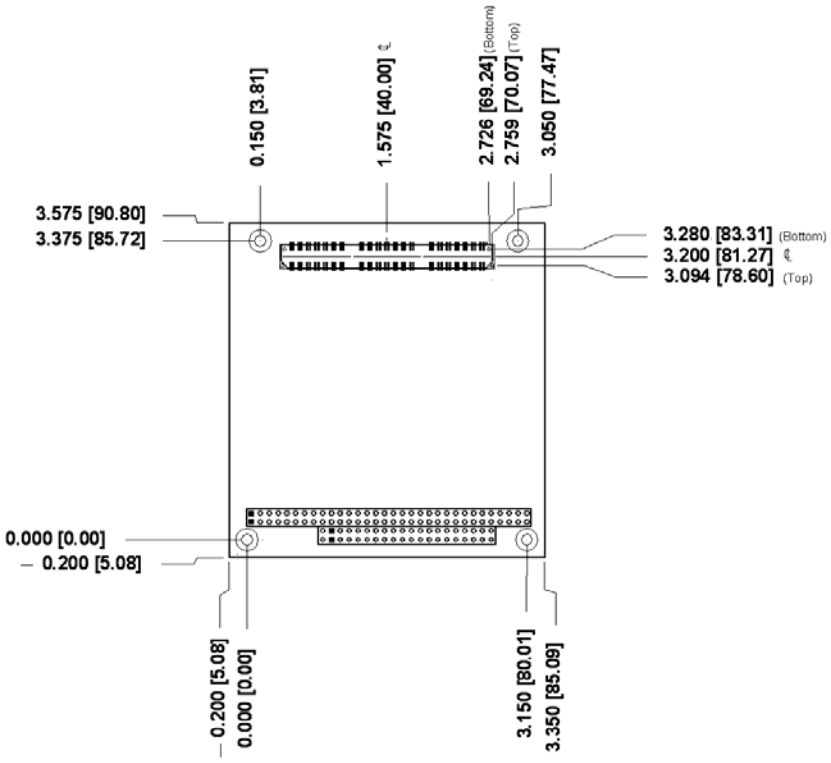
5.1 EPIC Express – Three-Bank Connector



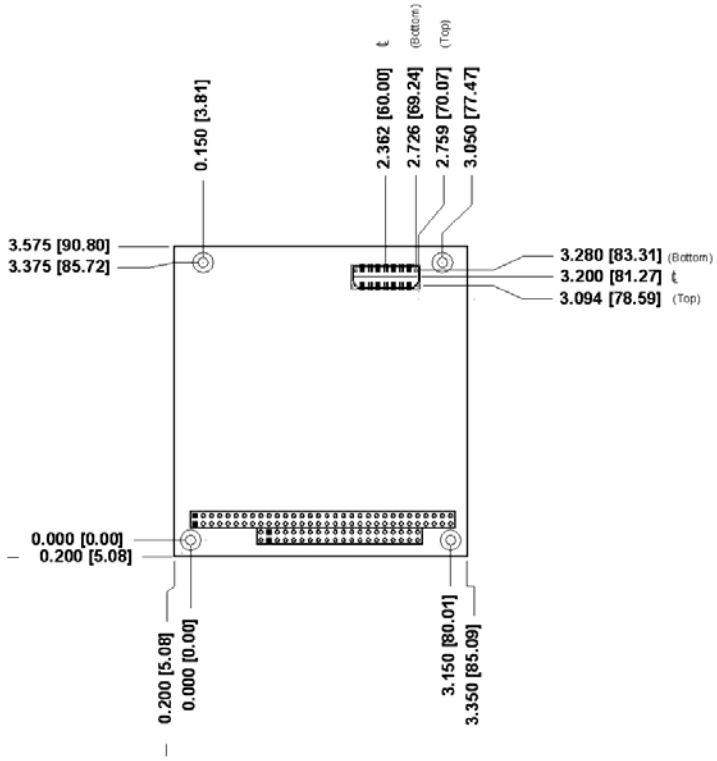
5.2 EPIC Express – One-Bank Connector



5.3 EPIC Express Expansion Card – Three-Bank Connector



5.4 EPIC Express Expansion Card – One-Bank Connector



*See the Reference section for links to the current EPIC and PC/104 Specifications.

6. ROUTING CONSIDERATIONS

6.1 PCI Express Electrical Perspective

EPIC Express, based on PCI Express signaling, requires careful consideration when laying out the SBC or expansion board. PCI Express is a 2.5 gigabit per second differential serial interface. With a maximum edge rate specified at 50 picoseconds, or 7 GHz, routing is critical. Even at realized real world edge rates of ~100 picoseconds, the utmost in attention to detail is required for a successful design.

There are many sources available that discuss both high speed printed circuit board design and PCI Express specific design guidelines. The following is no way any attempt to repeat this information, or instruct the designer in these areas. It merely touches on general guidelines that should be observed, as well as some EPIC Express specific design rules.

Any designer building an EPIC Express SBC or expansion product should refer to the PCI Special Interest Group for the PCI Express Specifications. The following is intended only to help the designer identify areas for special consideration and further research. This design guideline list should by no means be considered as a complete reference, only a reasonable starting point. Following these guidelines does not guaranty a successful design and no such guaranty is expressed or implied.

6.2 EPIC Express Routing Guidelines

Due to the high speed nature of PCI Express signaling, careful consideration must be given to the electrical design. When designing a printed circuit board for any extremely high speed differential signaling environment, the symmetry of the circuit is of utmost importance. Matching each segment pair length, matching left hand and right hand turns for the pair, placing vias or components symmetrically in the signal path, and routing the trace pair symmetrically to these features are critical to minimize impedance, reflection, and flight time mismatches that degrade signal quality at these frequencies.

Recommended Implantation Guidelines:

- 0.062” nominal PCB thickness
- 100 ohm +/- 20% characteristic differential impedance
- 0.005” trace width, 0.007” space between pairs
- 0.020” minimum space from differential pairs to adjacent conductors
- Match signals of differential pair as closely as possible, 0.005” max per board
- One via per card per signal plus one via each end for breakout
- Vias placed symmetrically in the differential pair path
- Capacitive coupling components placed as close as possible to transmitter and placed symmetrically in the differential pair trace path
- Match number of turns left and right, no sharp or 90 degree turns

- Microstrip routing only over solid planes. (No routing over breaks in planes)

Recommended Implantation Guidelines (continued):

- Stripline routing is not recommended unless using blind vias to eliminate stub
- Match lane to lane length within a link to +/-2.000" on SBC and +/- 0.500" on Expansion card
- Maximum lane length on a SBC is 11.500" component to connector
- Maximum lane length on an expansion card is 2.500" connector to component
- Maximum lane length on an expansion card is 0.500" to route up from bottom connector to the top connector as a totem pole pass-through

6.3 Power

The EPIC Express specification provides for power to be supplied through the Express connector on designated pins in bank one and bank two. Ground return is supplied via the center ground contact in each bank populated. It is highly recommended that switching type power supplies be used to generate any expansion card voltages necessary because of their excellent transient response and their inherently high efficiency.

The following table describes the maximum power available for each expansion module. The power available to the module stack is dictated by the SBC vendor for any given SBC. Power requirements in excess of the SBC's available power specification, or greater than those listed below for an individual expansion card, must be supplied by a secondary connector on the expansion card itself. This secondary power connector must conform to the PC/104 and PC/104-*Plus* specifications for component height above or below the board and connector overhang areas.

Expansion Card Power, One Bank Connector:

+5V	2 Amps per expansion card
+3Vaux	500 milliamps per expansion card

Expansion Card Power, Three Bank Connector:

+5V	5 Amp per expansion card
+3Vaux	500 milliamps per expansion card
+12V	500 milliamps per expansion card
-12V	500 milliamps per expansion card

* These current capacities are independent of the PC/104 connector ratings.

7. THE FUTURE OF EPIC Express

7.1 EPIC Express x16 VIDEO

The EPIC Express Specification formalizes all necessary electrical and connectorization concerns to implement PCI Express in a small, stackable form factor. The next generation single board computer will likely require very high bandwidth video for embedded applications as well.

Planning for a sixteen lane (x16) PCI Express video link specifically addressing the special requirements of EPIC Express is underway. The EPIC Express x16 Video Specification will bridge EPIC to very high performance video applications, leveraging the same low cost design and connector technologies utilized for EPIC Express.

8. REFERENCE DOCUMENTS

This document specifies the mechanical information and basic routing suggestions for EPIC Express. For the most current electrical and mechanical information concerning the EPIC, PC/104, PC/104-*Plus*, EBX, PCI and PCI Express Specifications, contact the references below.

For information about PC/104, PC/104-*Plus*, EBX, and EPIC

PC/104 Embedded Consortium
PO Box 78008
San Francisco, CA 94107-8008

Phone: 415-243-2104
Fax: 415-836-9094
Email: info@pc104.org
Website: pc104.org

For information about PCI and PCI Express

PCI Special Interest Group
5440 SW Westgate, #217
Portland, OR 97221
Phone: 503-291-2569
Fax: 503-297-1090
Email: administration@pcisig.com
Website: www.pcisig.com

For more information and updates about the EPIC Express specification,

Website: www.epic-express.org

If errors are found in this document, please send your written comments to:

Email: specinfo@epic-express.org